

12V input
Terminals

12VDC Bus Power FET Switches

ISL70100
Current
Sense

ISL70321
Power Sequencer

ISL70321

PG LED Indicators

Quad_Clock
Master + Slave
8 Clocks

ISL71218
KILL
Compar.

PWM_Controller VCCINT
+ Local Load Slammer

LDO MGTY
AVCCAUX
+ Local Load Slammer

LDO MGMT AVCC
+ Local Load Slammer

ISL71001 MGTY AVTT
+ Local Load Slammer

POL 5V BUS2

POL VCCO 50x,
 VCCO HDIO
 + Local Load Slammer

POL VCCAUX
+ Local Load Slammer

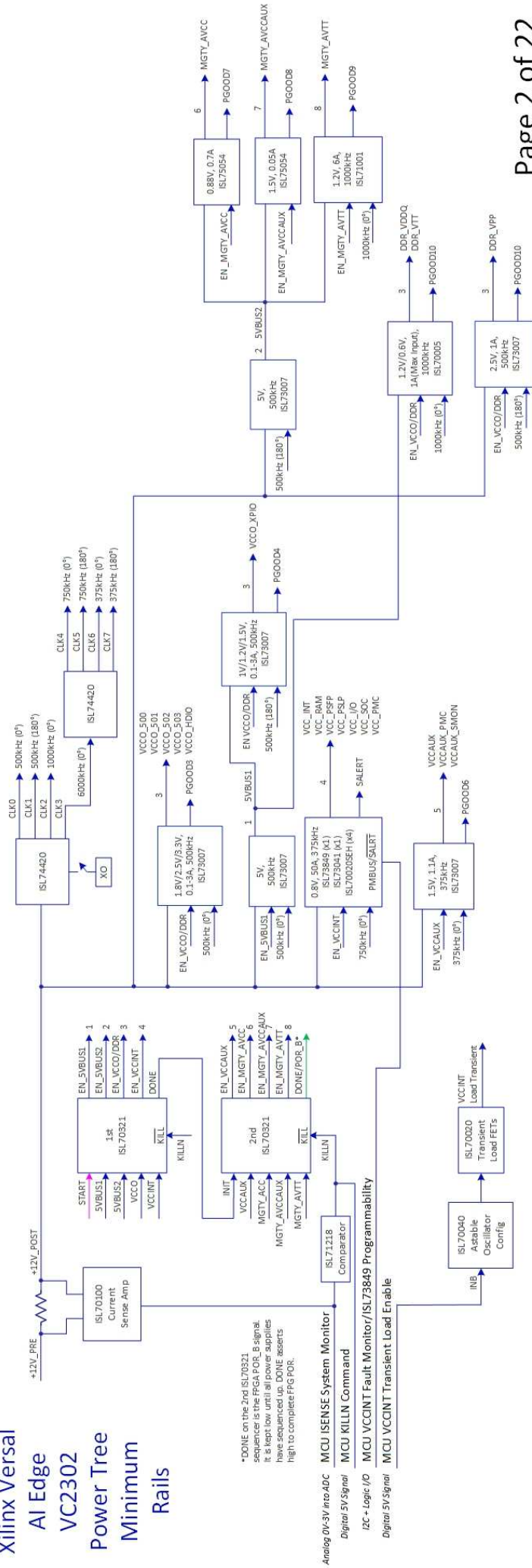
POL DDR Vpp
+ Local Load Slammer

ISL70005 DDR VDD, DDR VTT

POL '5V BUS1

POL VCCO XP10
+ Local Load Slammer

Xilinx Versal
AI Edge
VC2302
Power Tree
Minimum
Rails

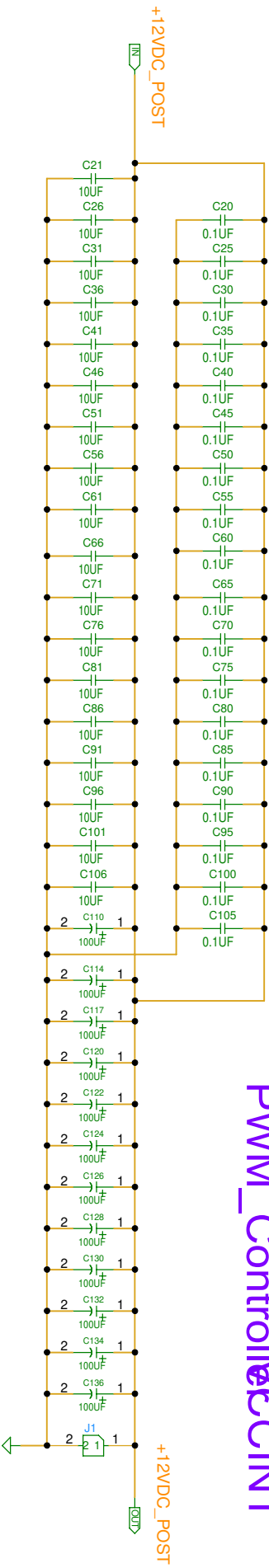


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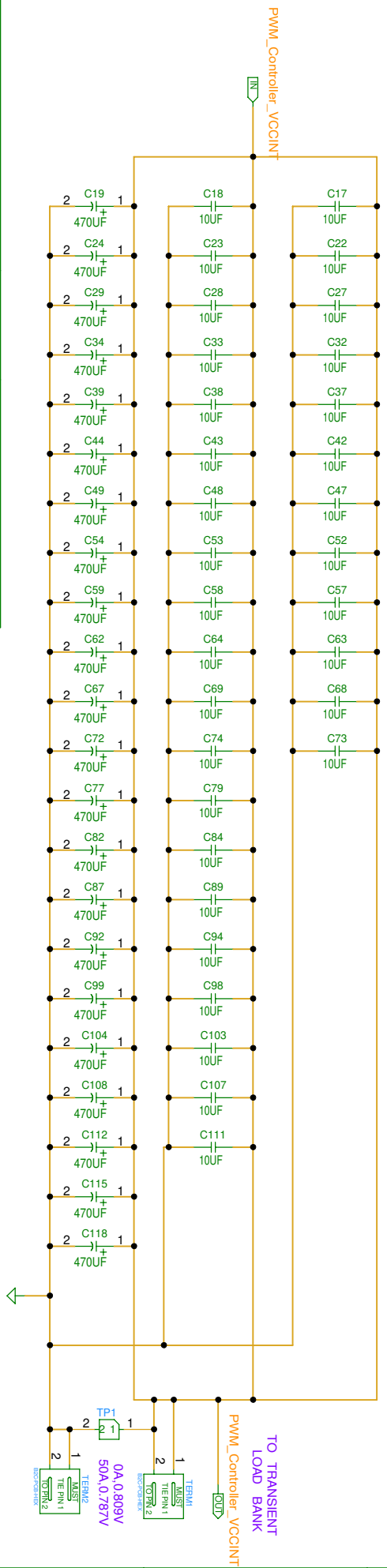
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UPDATED BY:	DATE:			
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INPUT CAPACITORS

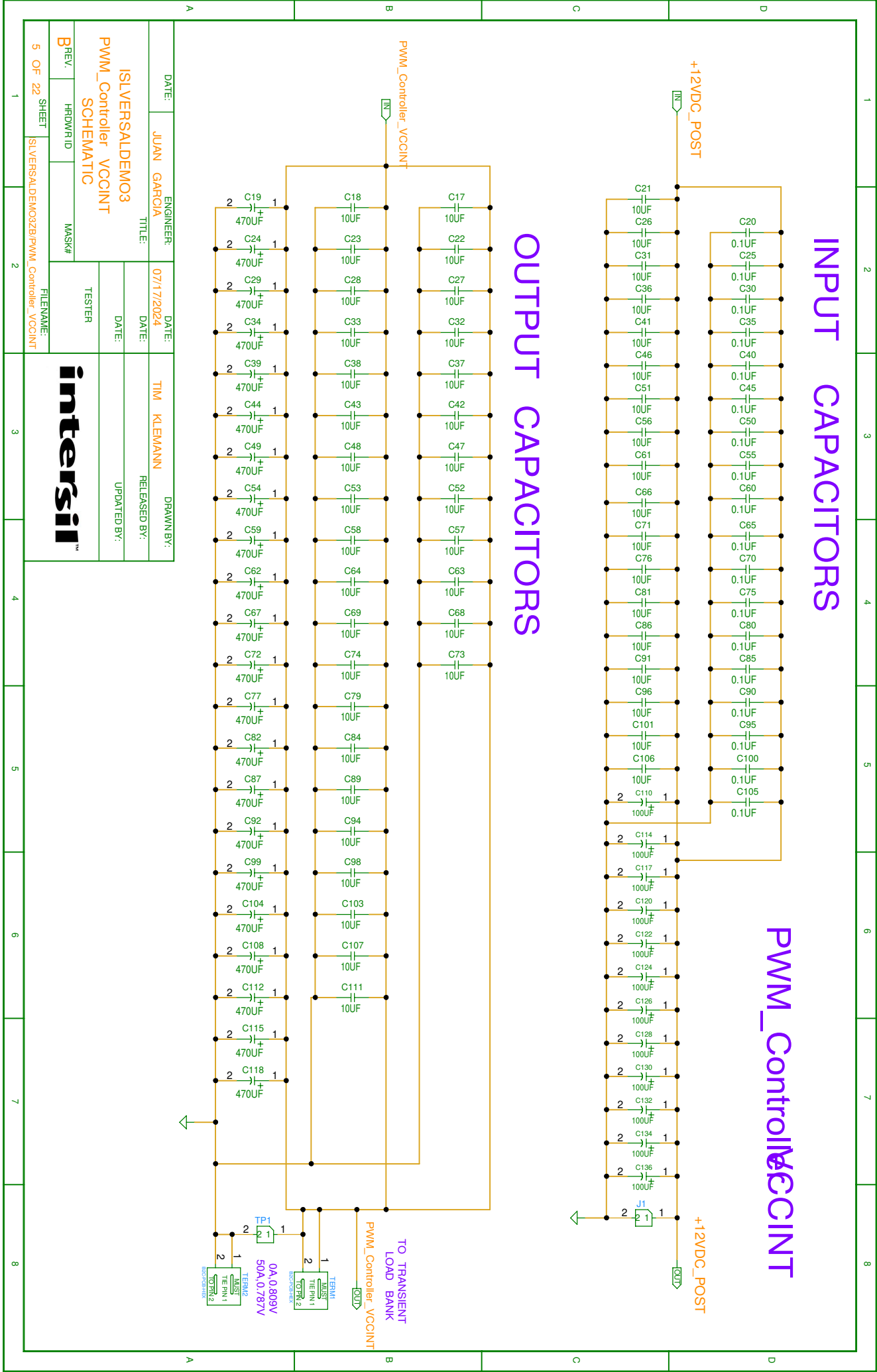


PWM_Controller_VCCINT

OUTPUT CAPACITORS

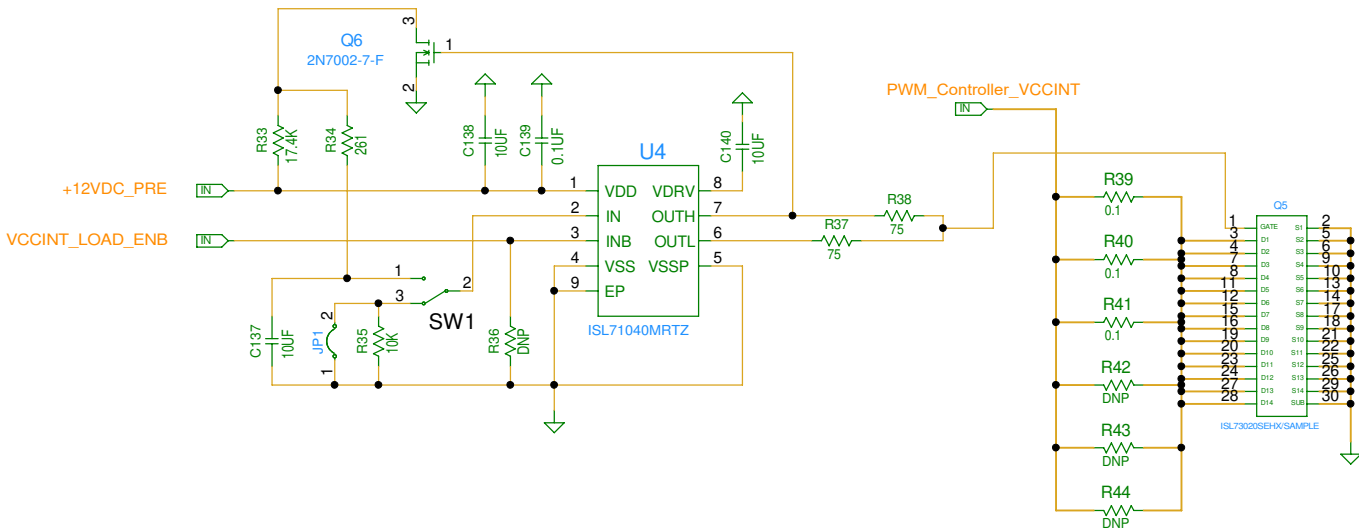



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TITLE:	ISLVERSALDEM03	DATE:	07/17/2024	RELEASED BY:	
PWM_Controller_VCCINT	SCHEMATIC	DATE:		UPDATED BY:	
BREV.	HRDWR ID	MASK#	TESTER		
5 OF 22 SHEET	SLVERSALDEM03B/PWM_Controller_VCCINT				

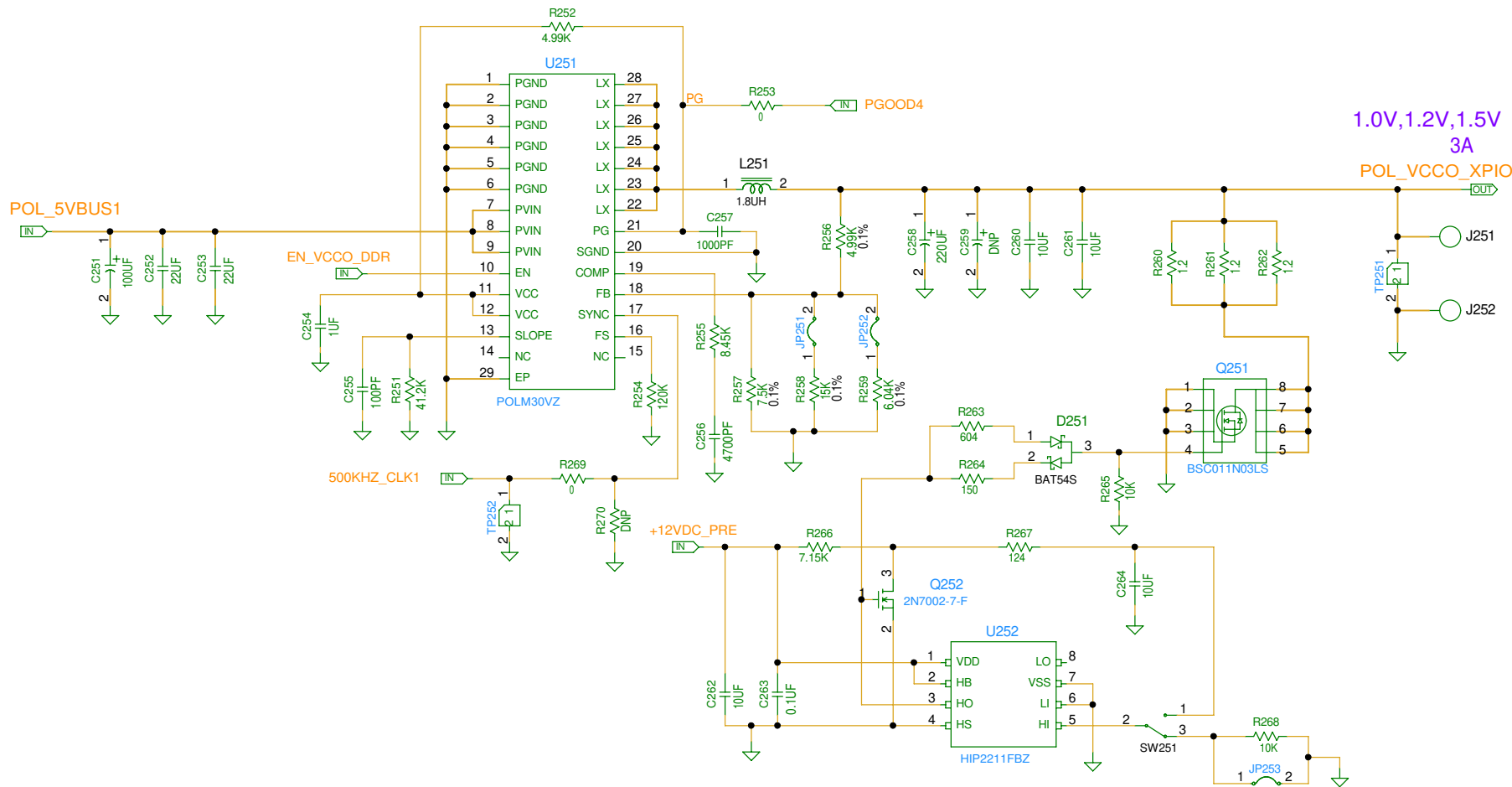


PWM_Controller VCCINT


TRANSIENT LOAD GENERATOR

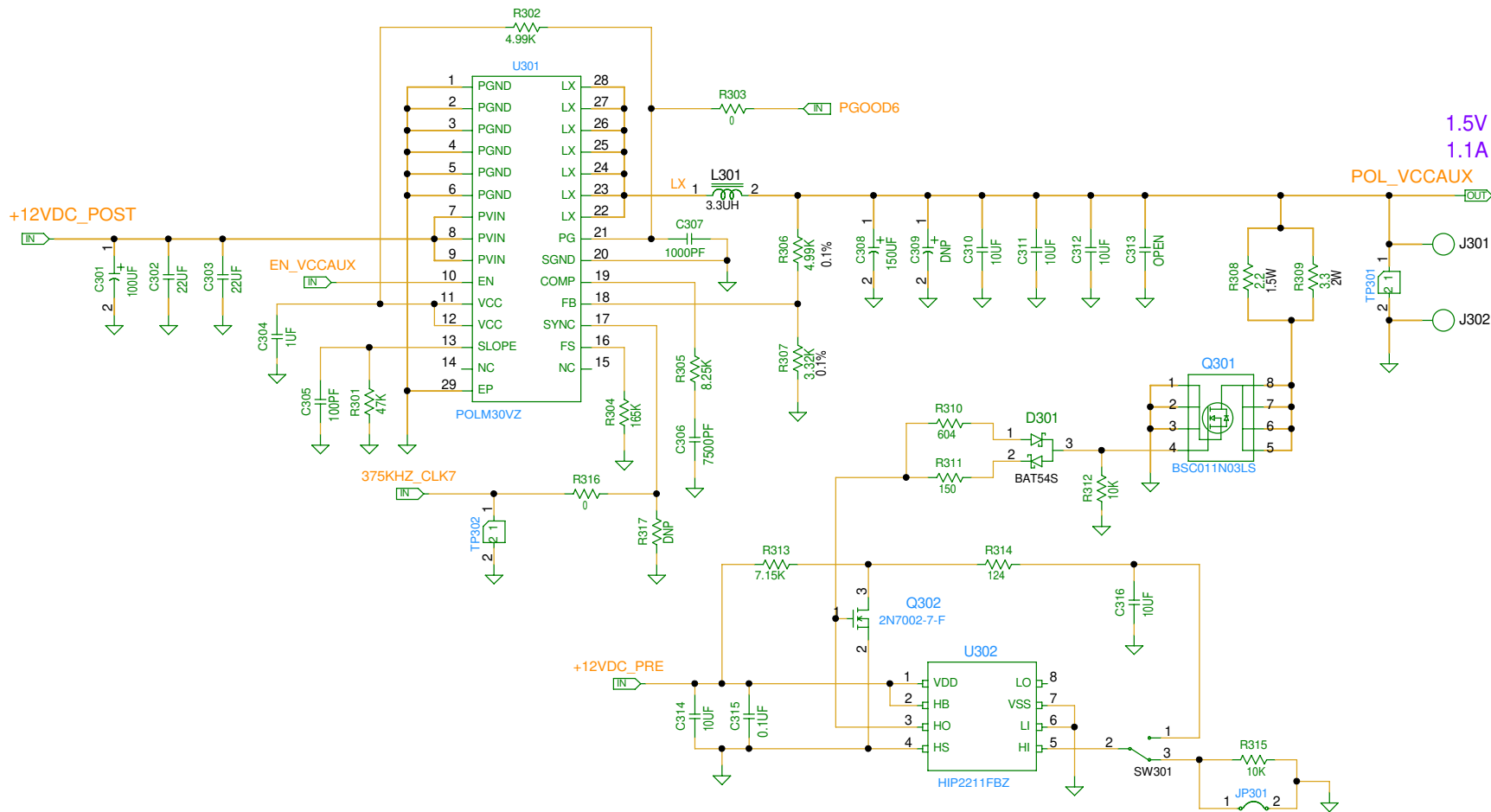


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POL VCCO XPIO

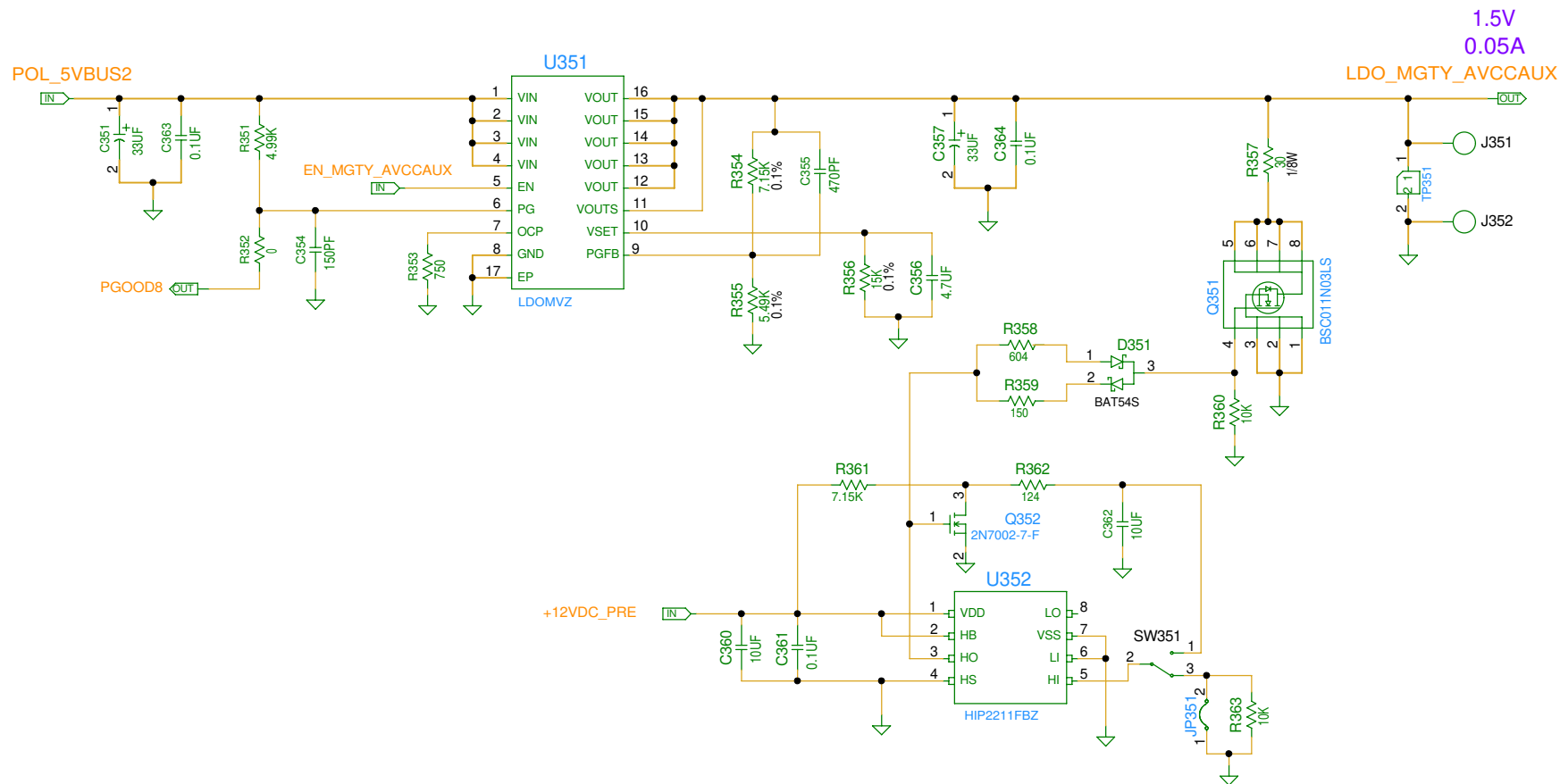
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UPDATED BY:	DATE:	TESTER	
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FILENAME: ISLVERDSALDEMO22B/POL_VCCO_XPIO		REV. B	
		SHEET 8 OF 22	



POL_VCCAUX
VCCAUX, VCCAUX_PMC, VCCAUX_SMON

DRAWN BY: TIM KLEMANN		DATE: 07/23/2024		ENGINEER: JUAN GARCIA		DATE:	
RELEASED BY:		DATE:		TITLE: <div>ISLVERSALEDEMO3 POL_VCCAUX SCHEMATIC</div>			
UPDATED BY:		DATE:					
<div>intersil™</div>		TESTER					
				FILENAME: ISLVERDSALDEMO22B/POL_VCCAUX		SHEET 9 OF 22	

MGTY_AVCCAUX LDO



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RELEASED BY:		DATE:		TITLE:	ISLVERSALDEMO3		
UPDATED BY:		DATE:		LDO	MGTY AVCCAUX		
				TESTER	SCHEMATIC		
				MASK#	HRDWR ID	REV.	B
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ISLVERSALDEMO3B/LDO_MGTY_AVCCAUX						10 OF 22	

POL_5VBUS2

PGOOD7

MGTY_AVCC

LDO

MGTY AVCC

U401

+12VDC_PRE

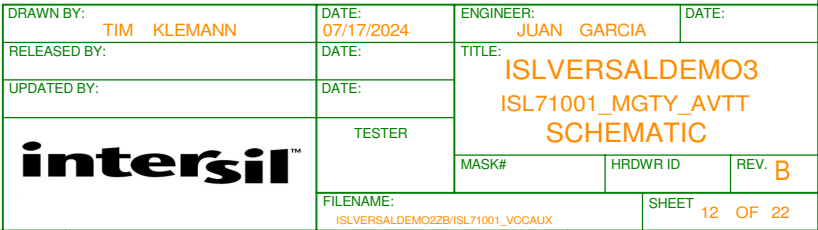
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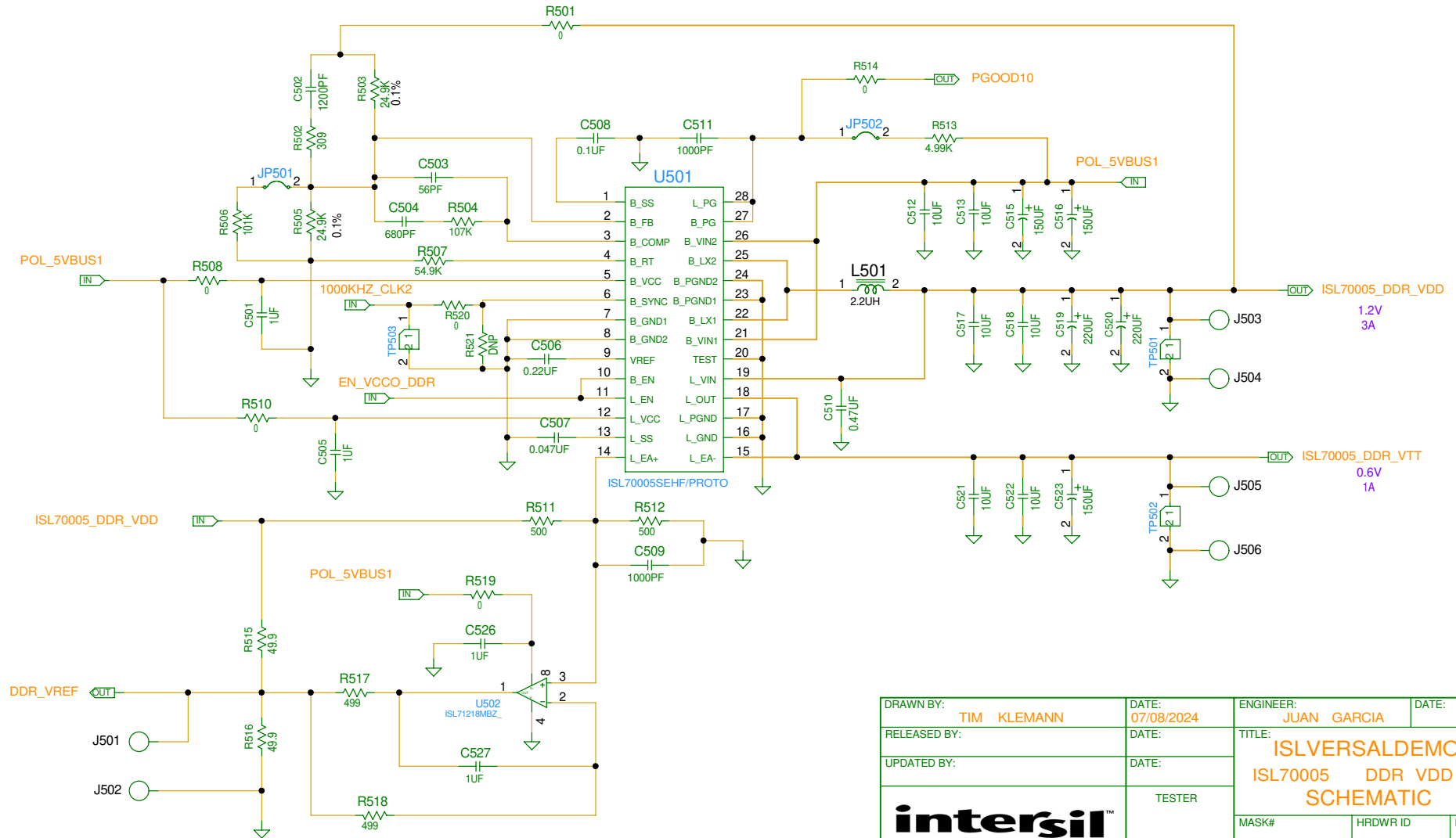
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LDO_MGTY_AVCC

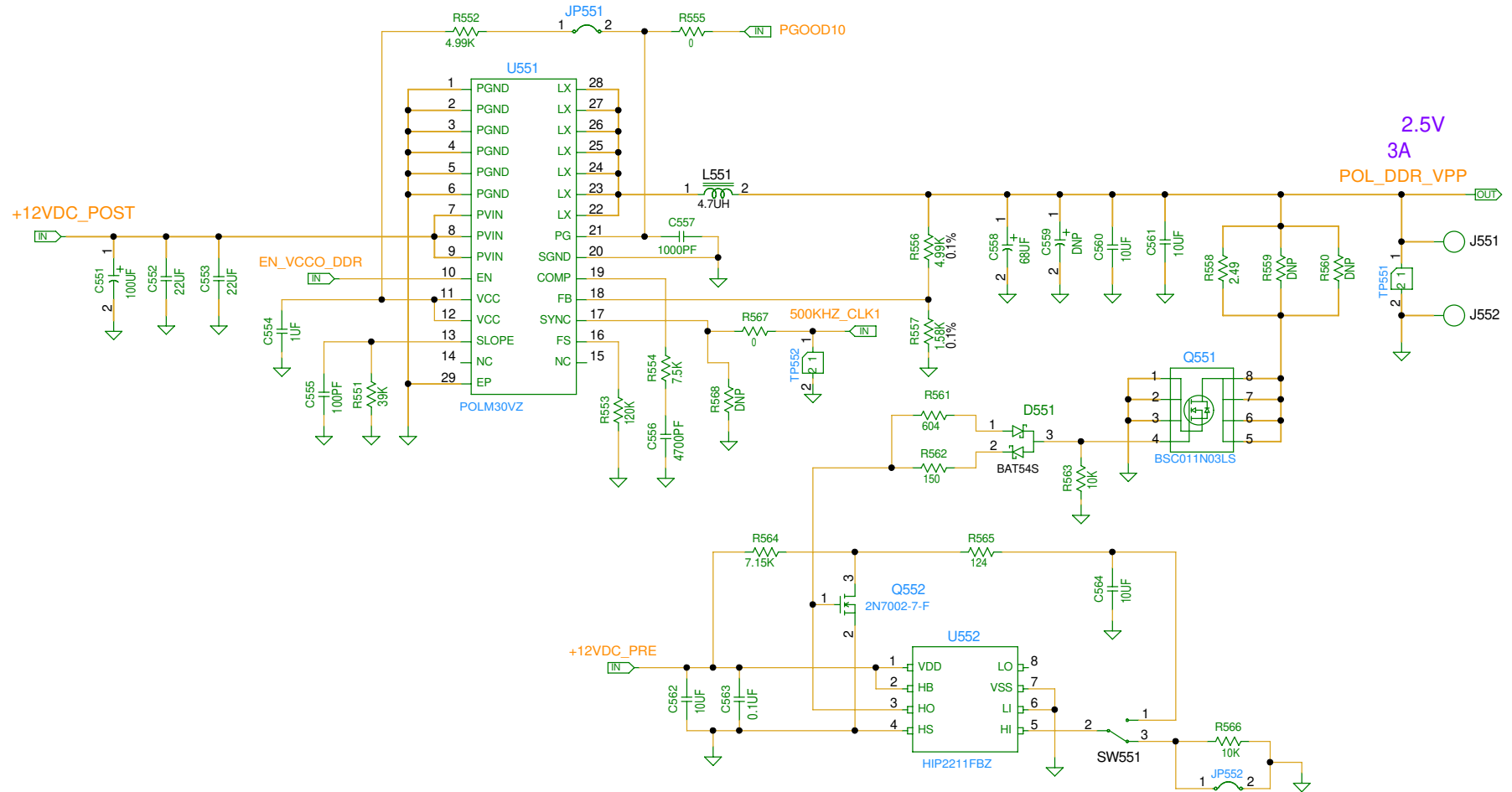
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UPDATED BY:	DATE:	TESTER	
interasil™		MASK#	HRDWR ID
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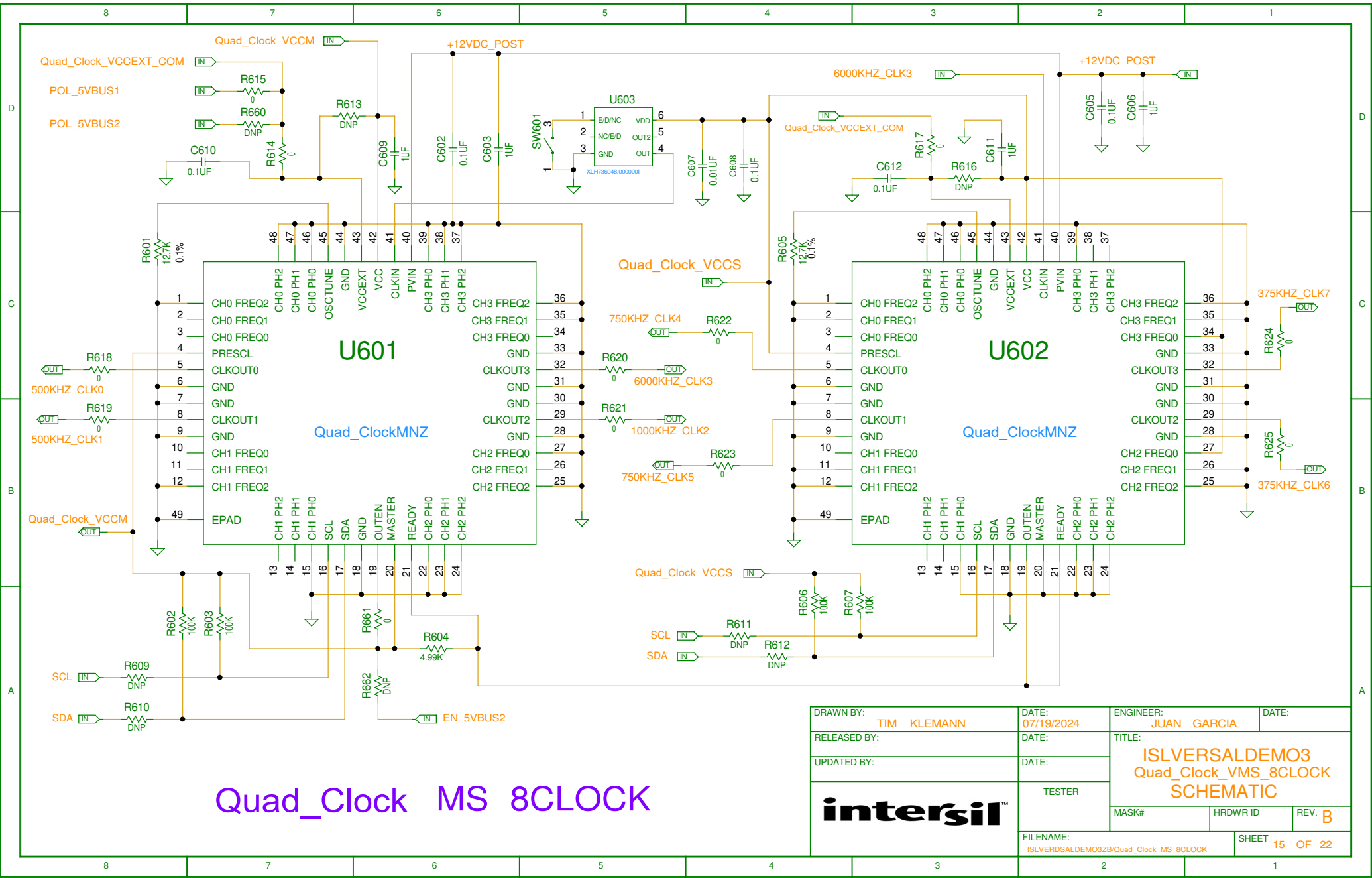
ISL70005 DDR VDD VTT



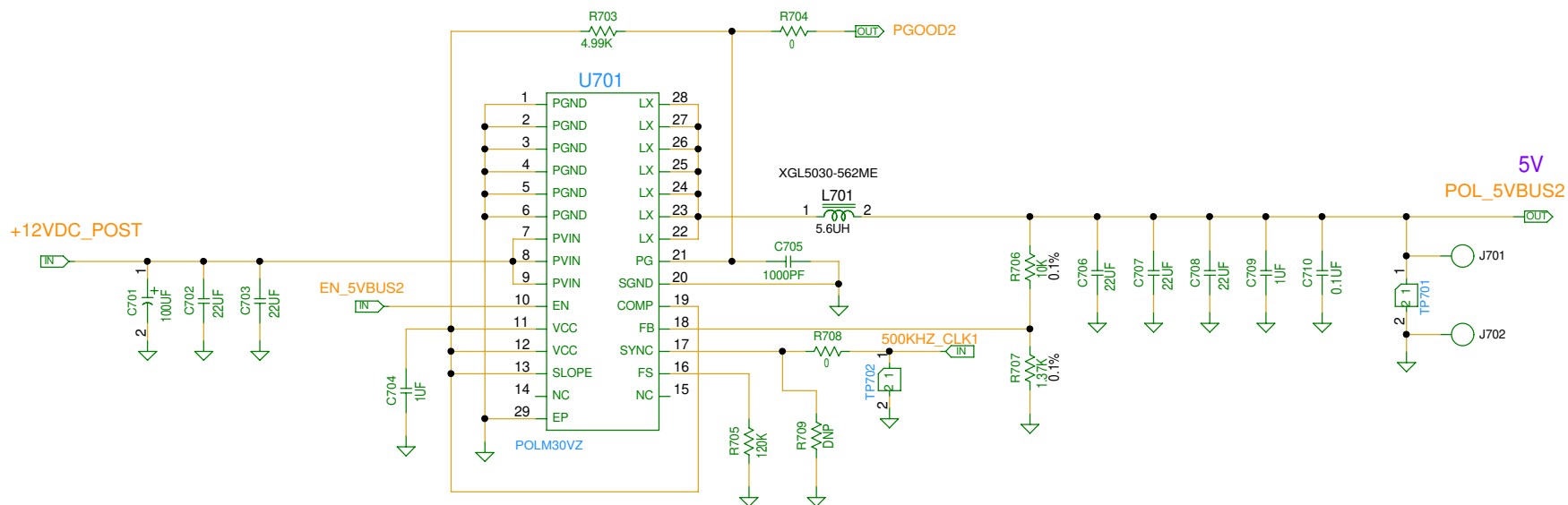
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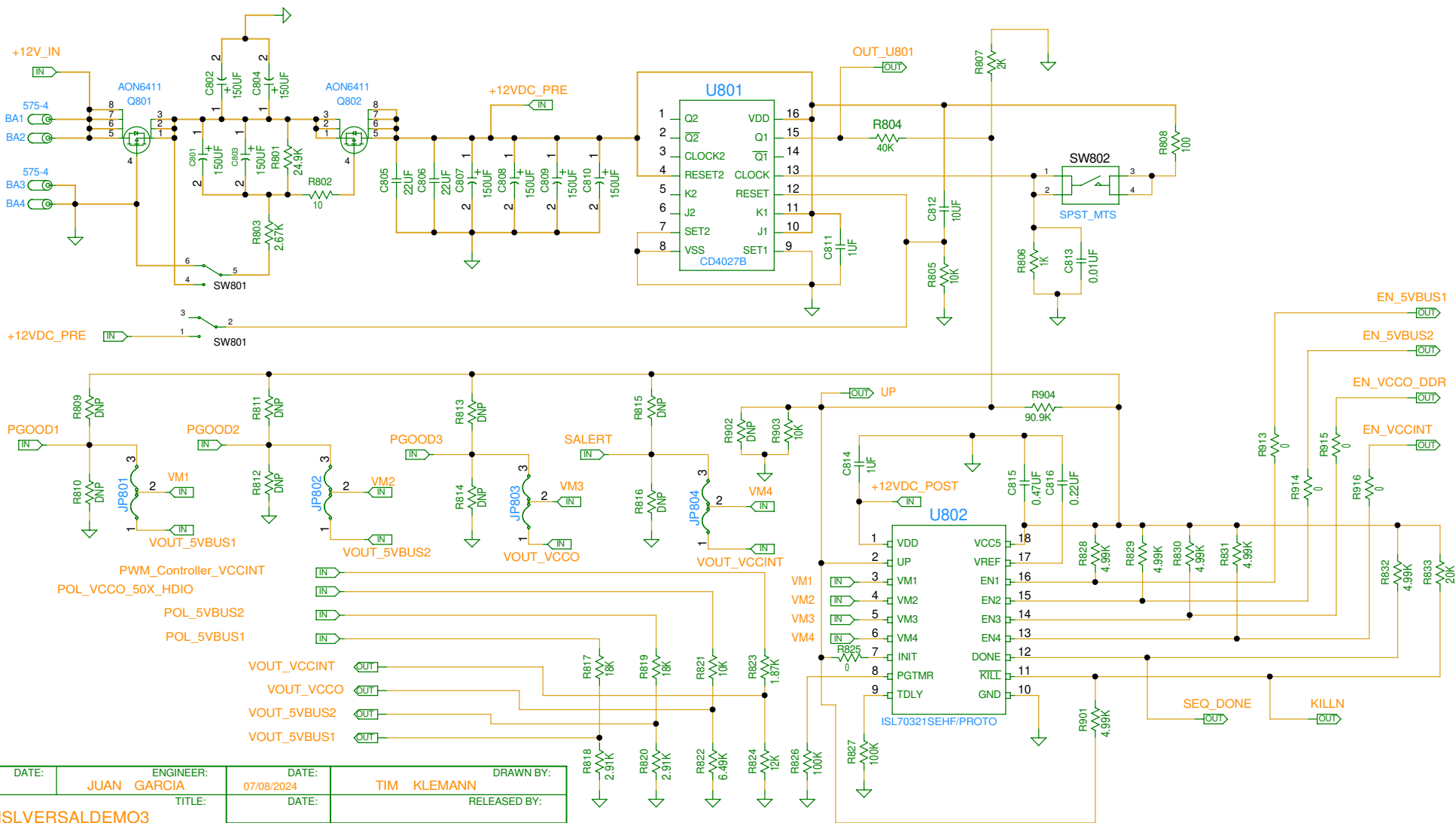
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intelsil™		MASK#	HRDWR ID
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SHEET 15 OF 22			



DRAWN BY: TIM KLEMMANN		DATE: 07/08/2024	ENGINEER: JUAN GARCIA		DATE:	
RELEASED BY:		DATE:	ISLVERSALDEMO3 POL 5V BUS2 SCHEMATIC			
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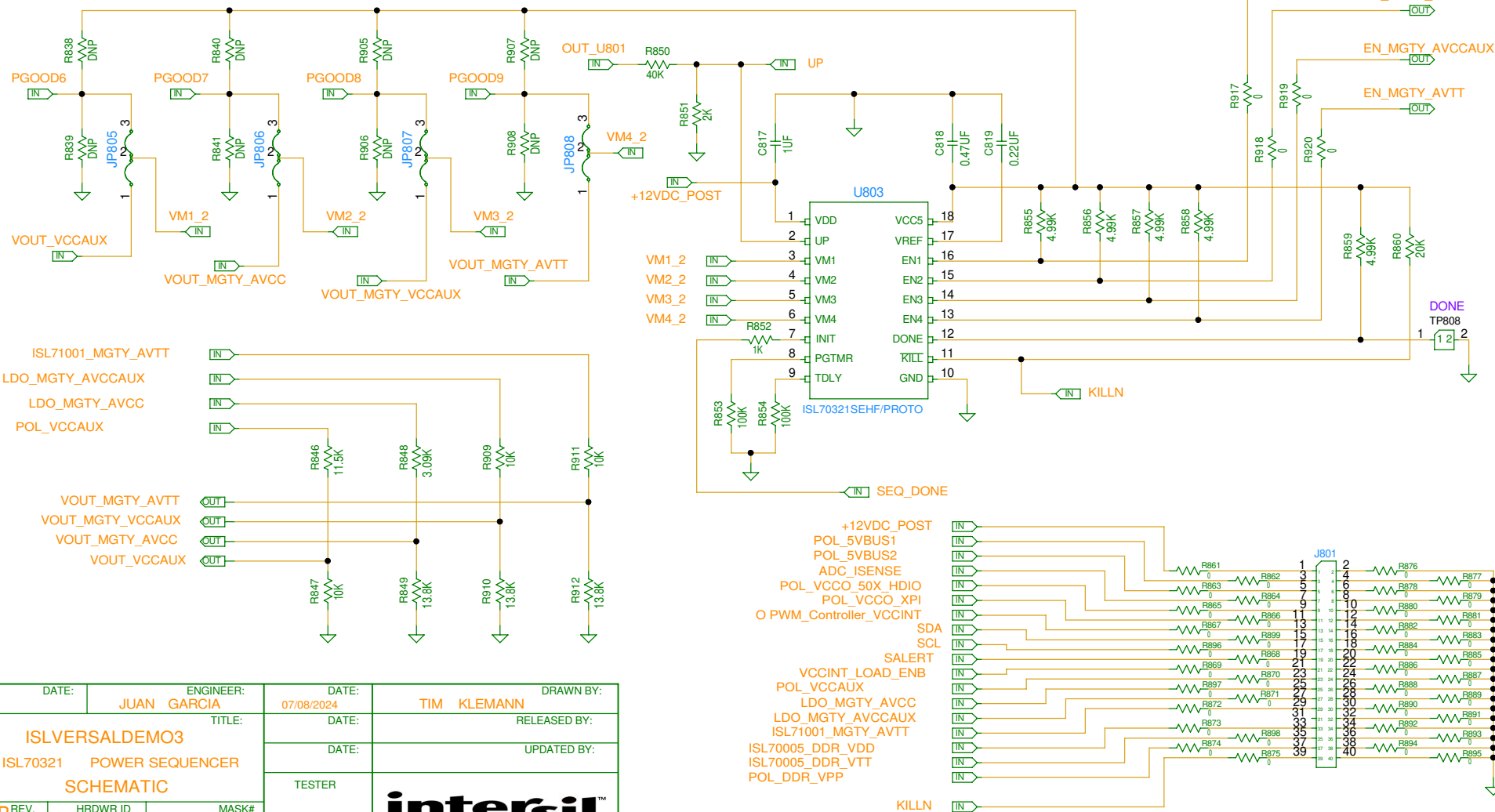


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		JUAN GARCIA		07/08/2024		TIM KLEMMANN	
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				DATE:		UPDATED BY:	
				TESTER			
B REV.		HRDWR ID		MASK#			
18 OF 22 SHEET				FILENAME:			
				ISLVERDEMO3ZB/ISL70321_POWER_SEQUENCER			

intersil

ISL70321 POWER SEQUENCER 1 +12V BUS POWER SWITCHES

ISL70321 POWER SEQUENCER 2 + 40-PIN CONNECTOR

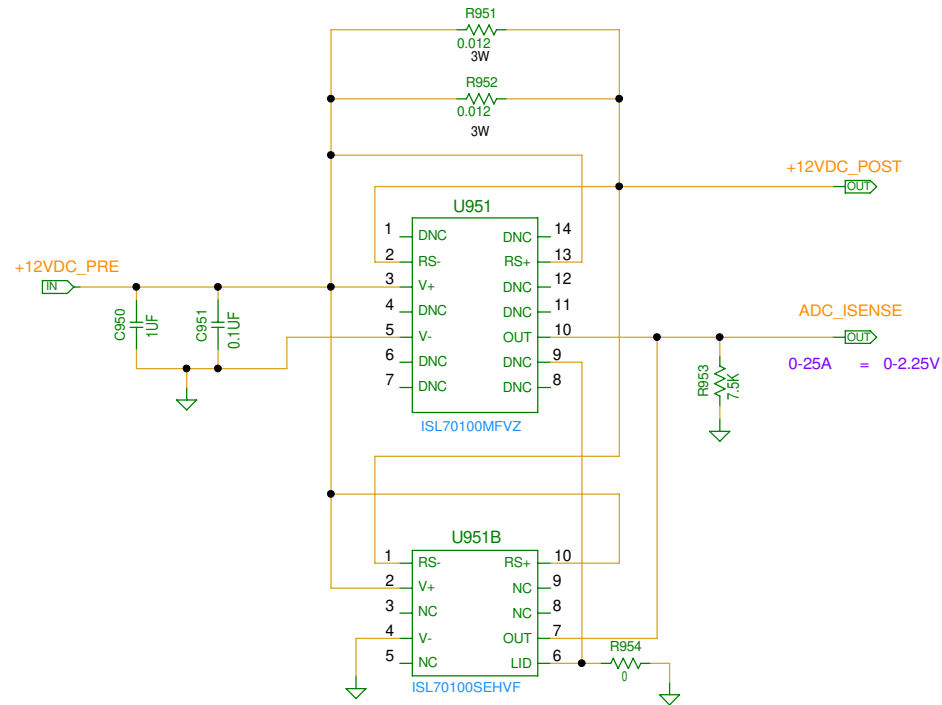


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	JUAN GARCIA	07/08/2024	TIM KLEMMANN
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SCHEMATIC		DATE:	UPDATED BY:
TESTER			
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intersil™

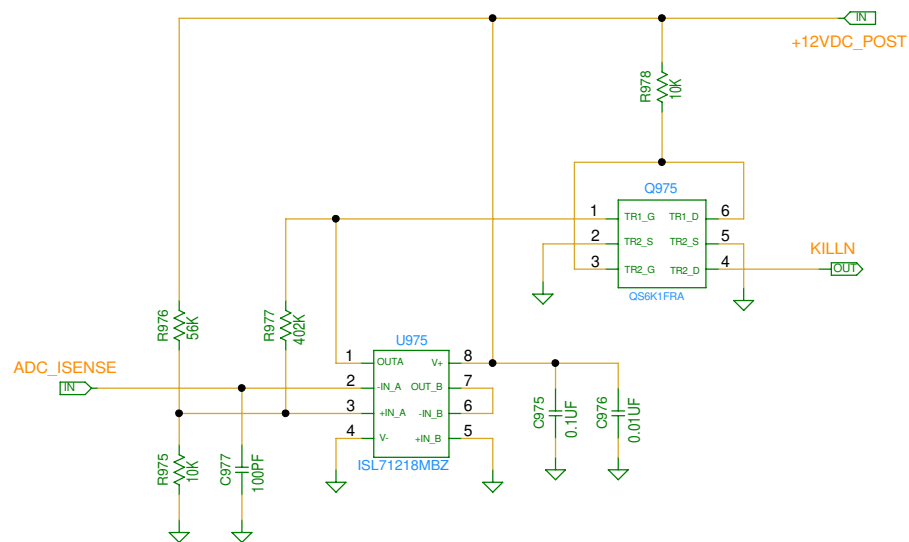
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SCHEMATIC
B REV. 19 OF 22 SHEET
ISL70321_POWER_SEQUENCER


ISL70100 CURRENT SENSE



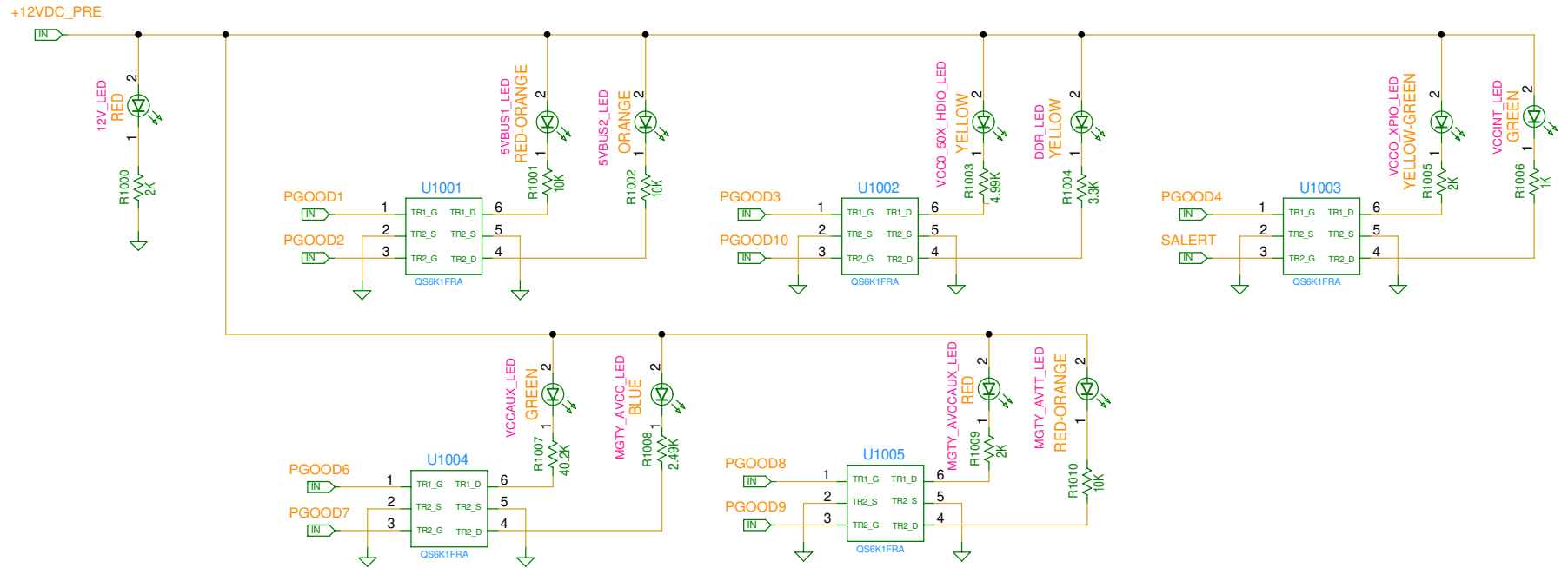
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ISL71218 KILL COMPARATOR



DRAWN BY: TIM KLEMANN		DATE: 07/08/2024		ENGINEER: JUAN GARCIA		DATE:	
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POWER LED INDICATORS



DRAWN BY: TIM KLEMANN	DATE: 07/08/2024	ENGINEER: JUAN GARCIA	DATE:
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UPDATED BY:	DATE:		
intersil [™]		TESTER	REV. B
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